3D Electro-Thermal Study for Reliability of Automotive Power Vertical MOSFET Using COMSOL Multiphysics

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Abstract: In this paper 3D electro-thermal FE Model using COMSOL Multiphysics software of power vertical MOSFET used in the automotive industry is presented. This model is used to analyze the effects of bonding wire lift off defect and to study the influence of metallization thickness and number of bonding wires on the electrical and thermal behavior of the power device. The maximum temperature enables the evaluation of the reliability of the power component. Such modeling is useful for optimization of structure design to guarantee a longer lifespan.

Keywords: Bonding wire lift off, debiasing effect, metallization, ultra-low on-state resistance.

1. Introduction

Due to the high degree of integration and car applications that impose very constraining conditions on the power components, new electro-thermal simulation tools are required to improve the design of components and ensure longer lifespan. Ambient temperature, or that generated by self-heating creates important thermomechanical constraints which induce defects in the structure (welding, bonding wire lift off, metallization reconstruction, delamination) which affect the electrical functions progressively [1, 2]. The sequence of events which follow the emergence of these defects is very important, and strongly conditions the occurrence of failure and finally the breakdown of the power device. These events are very often related to electro-thermal coupling phenomena in the chip and its nearby environment. These events depend particularly on technology and the design (thickness of the layers, position and number of bonding wires, electrical behavior of elementary cells. . .).

This paper deals with finite element modeling (FEM) of ultra-low on-state resistance power device using COMSOL Multiphysics software. The vertical MOSFET power switch used in the automotive industry is considered to sustain current up to 150 A on a 2-mΩ on-state resistance device. Its ultra-low on-state resistance allows it to be crossed by high current. It is impossible to simulate the microscopic electrical effect of each MOS transistor cell with a F.E. model. In spite of this limitation, it is possible to simulate the „fully ON" behavior of the transistor which is the dominating heat loses during a short circuit mode.
The modeling suggested in this paper represents a step in the electro-thermal investigation of the ON state behavior of an aged component disrupted by the defect of bonding wire lift off and the study of the influence of metallization thickness and number of bonding wires on the electrical and thermal behavior of the power device. Maximum temperature results obtained from an electro-thermal simulation are mandatory to evaluate the reliability of a power device [3].

2. F.E. Model of power device

Power device model is achieved with COMSOL Multiphysics software using a 3D electro-thermal element type that has two dependent variables, voltage and temperature. The power component consists of power chip that dissipates heat during its operation, two lead frames that are used to evacuate the heat and eight parallel aluminum bonding wires which connect the aluminum metallization layer to the copper lead frame. The component is geometrically and loads symmetric, so we considered that it"s sufficient to model half of the structure to describe the total behavior of the component. The power device is shown in Figure 1.

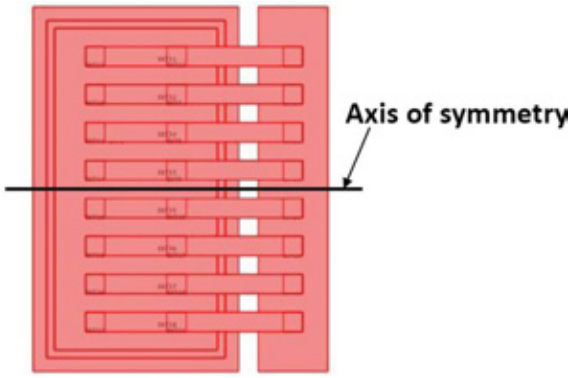

Figure 1. Power device.

In electro-thermal simulation, it is necessary to consider the variation of the resistivity of the active layer of the component with temperature, because it is the dominant resistance in the model and has the largest variation with temperature [4]. All the other material resistivities are considered to be constant with temperature because their influences and their variations are limited over the temperature range of interest in electronics (20–200 °C). All thermal properties of materials are considered to be constant with temperature for the same reasons as aforementioned.

The issue raised when attempting to obtain the FEM of the power device is the scale difference between the thickness of layers making up the chip (micrometer) and its dimensions (millimeter). Layer thickness varies from 4 to 500 µm. Model length is approximately 9000 µm and width 4000 µm. Model meshing is the main difficulty given the micrometer and millimeter scale dimensions of the layers. Thin layers need to be fine-meshed but for reasonable simulation time, the model size must be minimized. To resolve this issue, a smart meshing is undertaken. The free mesh parameters box in the Mesh menu was used and the parameters have been varied until a compromise between the number of elements and precision is obtained.

Boundary conditions on the FEM are applied to the bottom surface of both copper lead frames. A zero volt potential is applied to the source lead frame (the one connected to the aluminum wire) and current density (J_{DS}) equal to 634 A/cm^2 is imposed on the bottom of the drain lead frame (under the silicon die). The thermal boundary conditions are forced convection. Convection coefficients (h) equal to 2000 W m^{-2} K^{-1} are applied to the bottom surface of both copper lead frames and external temperature (T_D,T_S) are equal to 20 °C. Transient simulations are made during 50 ms with a step of 10 ms. The number of elements for the model is approximately 36560 and computational time is about 7minutes. The F.E. Model description is shown in Figure 2.

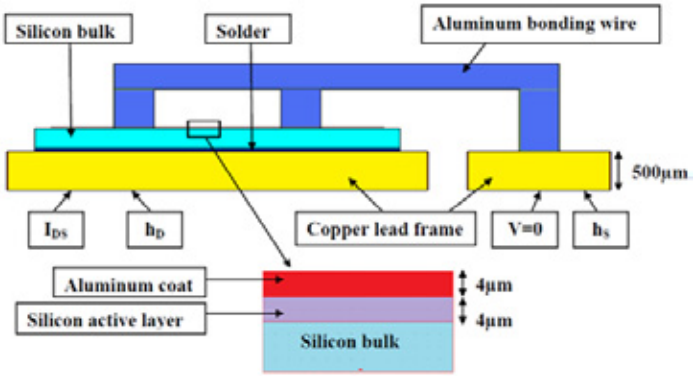

Figure 2. FEM description.

Simulation conditions set to model induce a maximum temperature of 170 °C which is the higher functioning temperature limit of MOSFET device. Thus, the power device presented in this paper is designed to sustain a short circuit mode that generates 400 W/cm^2 during 50 ms. Temperature and voltage distribution results on device for such functioning conditions across half of the device are presented in Figure 3. Maximum voltage drop given by simulation is 0.748 V. Therefore, R_{ON} can be computed by dividing maximum voltage by imposed current. The result is 4.98 mΩ for half of the real structure and therefore for the entire device is 2.49 mΩ.

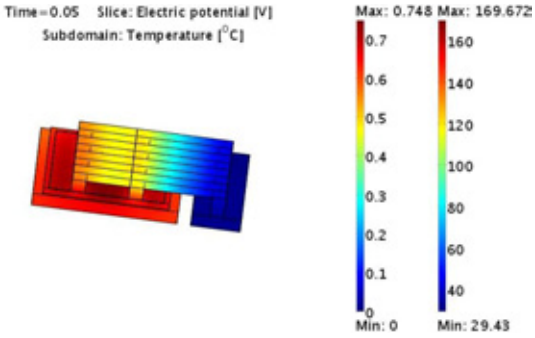

Figure 3. Temperature and voltage distribution on power device (T_{max}= 50 ms, for J_{DS}= 634 A/cm^2).

3. Electro-thermal simulation of power device damages

One of the most basic failure mechanisms of power devices comes from bonding wire lift off. The root cause of this failure is the difference in thermal expansion coefficient between silicon and aluminum, which induces a high level of thermo-mechanical stress each time the power undergoes a temperature variation. Such repeated thermomechanical stress generates plastic deformation between source metallization and bonding wires and leads at the end to bonding wire lift off. This failure mechanism has been simulated and temperature results are presented in figure 4 for the same electrical and thermal boundary condition as mentioned in the previous section. It can be observed from Figure 4 that the maximum temperature has increased by 69 °C and is located next to the only contact between the bonding wire and the top metallization. This significant increase in temperature is an electro-thermal effect arising from the focalization of current density near to the only contact between bonding wire and top metallization. This focalization is induced by top metallization debasing effect that changes the distribution of current density through the surface of the power device [5]. A maximum temperature of 239 °C is not acceptable as it leads to early failure of the device. The next section presents a solution to this problem, which involves increasing metallization thickness.

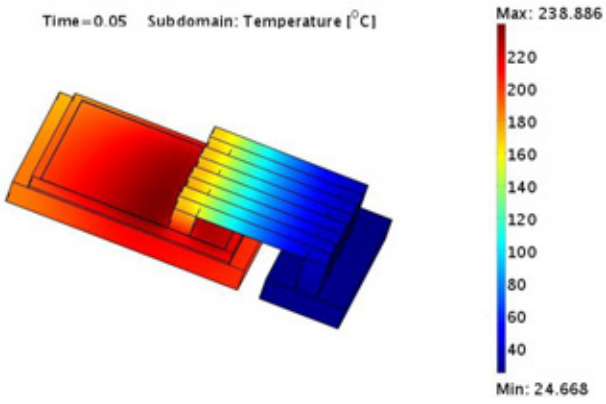

Figure 4. Temperature distribution on power device (T_{max}= 50 ms, for J_{DS}= 634 A/cm^2).

Additionally, the impact of the number of failed wires has been simulated. The maximum temperature increases with the number of failed wires. Temperature results of the number of failed wires are presented in Table 1.

Number of failed wires	Maximum temperature (°C)
0	170
1	178
2	190
3	402
4	239

Table 1. Maximum temperature on power device as a function of number of failed wires

4. Electro-thermal simulation of metallization thickness

A way to minimize the effect described in the previous section is to increase top metallization thickness that will reduce top metallization debiasing effect. The previous simulations were performed on a device with a metallization thickness of 4µm. Several simulations were done to quantify the effect of top metallization thickness on the maximum temperature of the power device. Figure 5 shows temperature results for a metallization thickness of 30 µm. It can be observed from Figure 5 that the maximum temperature is 187 °C, which corresponds to a decrease of 52°C compared to the device with 4 µm metallization thickness. Thus impact of failed wires is minimized.

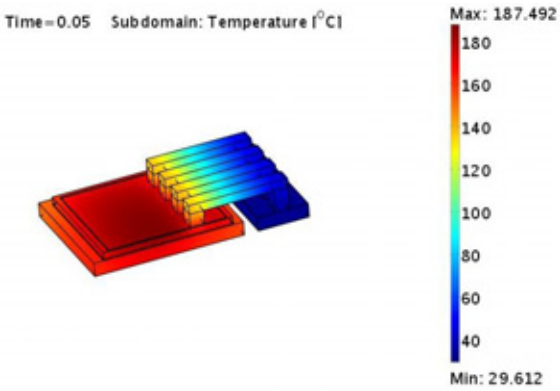

Figure 5. Temperature distribution on power device (T_{max}= 50 ms, for J_{DS}= 634 A/cm^2).

However, too thick top metallization is not realistic. It is interesting to use the finite element simulation to determine the minimum thickness of metallization necessary to reduce significantly temperature increase from bonding wire lift off. Figure 6 presents the maximum temperature of the device versus the thickness of metallization for the same operating conditions.

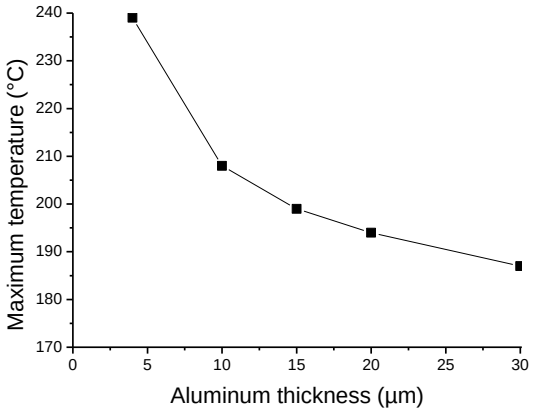

Figure 6. Maximum temperature on power device as a function of metallization thickness (T_{max}= 50 ms, for J_{DS}= 634 A/cm^2).

5. Conclusions

In this paper, a F.E. model of power vertical MOSFET with an ultra-low on-state resistance has been presented. This model is used to investigate 3D electro-thermal coupling effects. The importance of electro-thermal simulation to evaluate the reliability of a power device has been shown. The effects of bonding wire lift off and number of wires on the device transient electro-thermal behavior are investigated during a short circuit mode. Increasing metallization thickness is a solution given to limit temperature increases due to failure mechanism such us bonding wire lift off.

6. References

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7. Acknowledgements

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