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COMSOL based simulation of optical response in Si microline array based broadband photodetector fabricated on Silicon-On-Insulator (SOI) wafers

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Outline

- **Motivation / Science issues**
- **Pros and cons of work**
- **Device fabrication process and Electron Microscope Characterization**
- **Results and discussion**
- **COMSOL simulation**
- **Conclusion**

Motivation / Science issues

Our proposal

- We propose to make array of Si microlines (~1 μm wide) fabricated by a top-down process that is compatible with wafer level processing.

- Make Metal-semiconductor-metal (MSM) photodetectors from the Si microlines.

- Achieve a large responsivity (R) larger than that available in commercial p-n detectors (0.6 A/W) although less than that in a single Si NW device (10^4 A/W).

Pros and cons of the work

1. Fabrication of array of microlines of Silicon using SOI is a new technology which is not only compatible with wafer scale processing but also turns out to be an adoptable road map for translation.

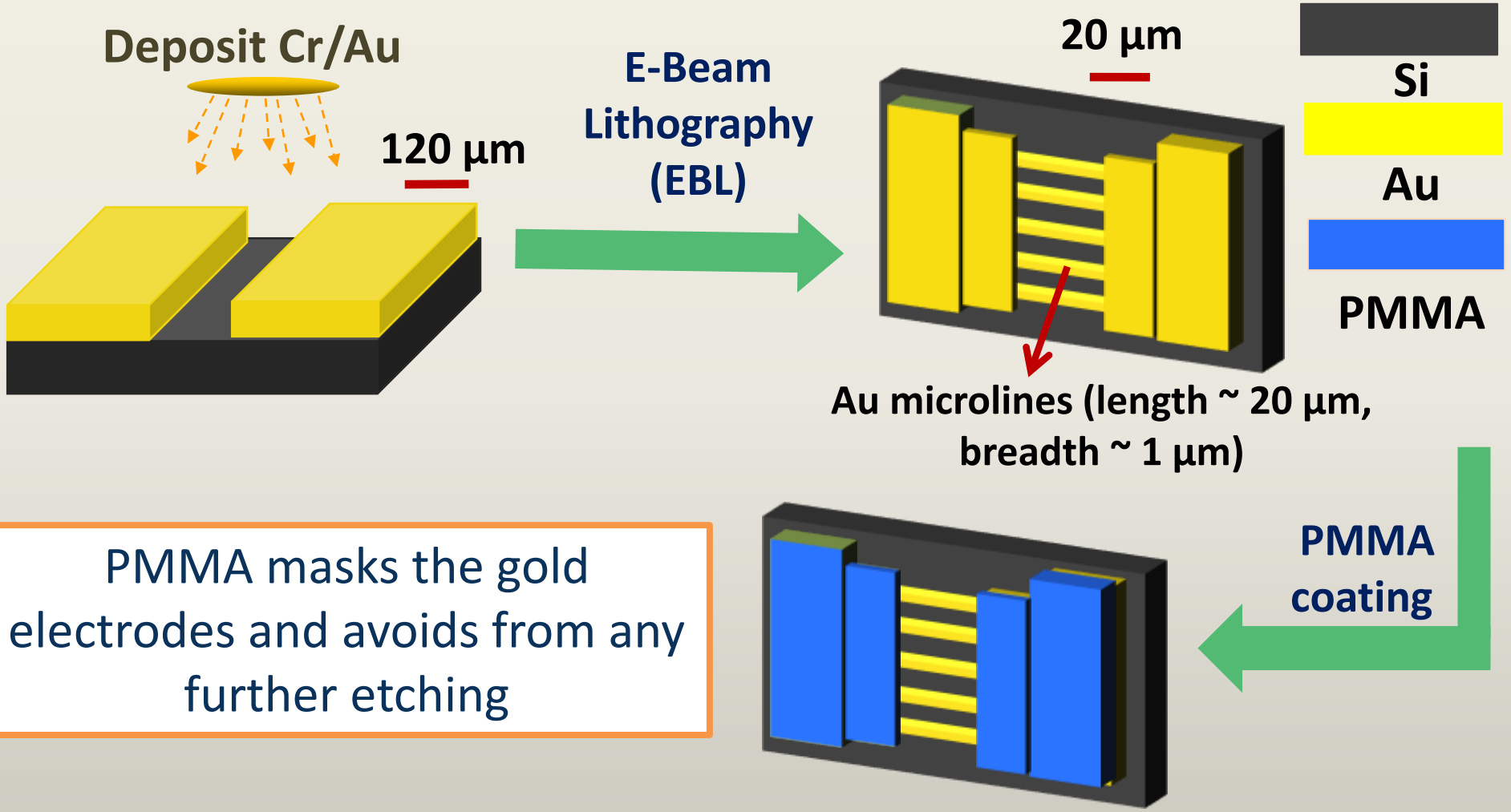
2. Growth of such type of arrays of microlines (planar) on wafers can be readily coupled to established batch processing tools.

3. The Responsivity (R) is an order higher than the commercially available 1A/W detectors.

Price paid

R will get limited to ~10-20 A/W although much larger than currently available 0.6 A/W in commercial p-n diode detectors.

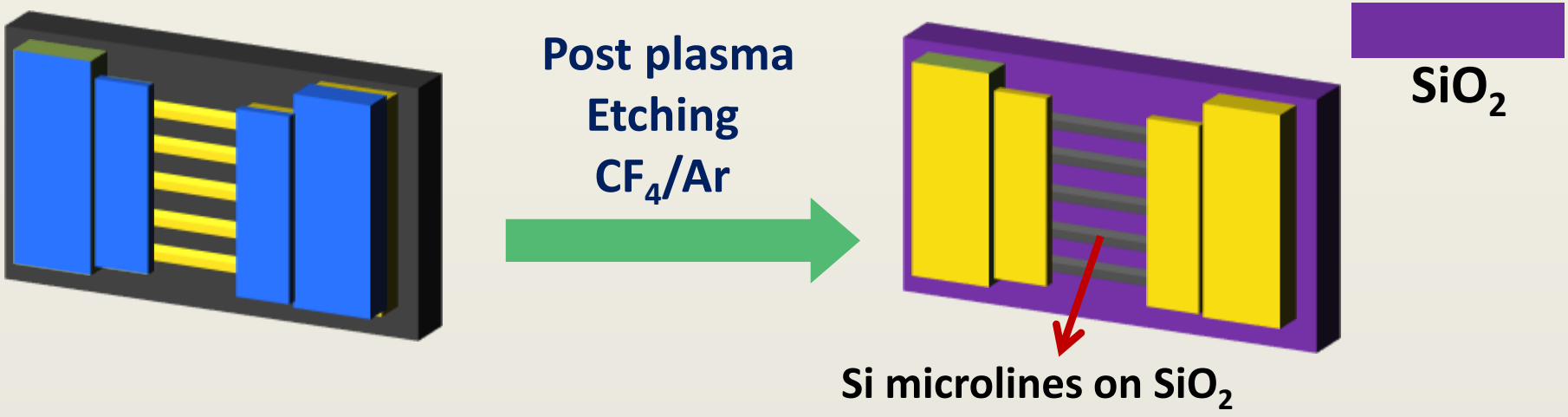
Device fabrication process



PMMA masks the gold electrodes and avoids from any further etching

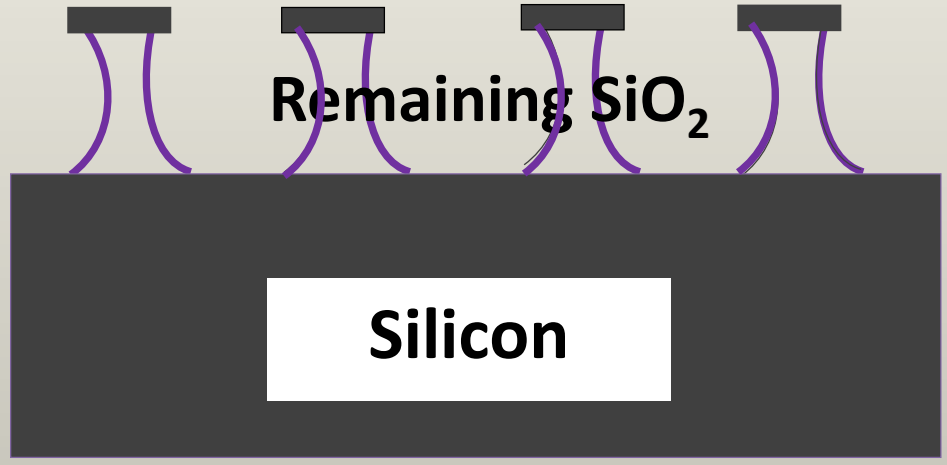
The Au lines are used as mask. Thickness (50 nm) is such that the process of etching removes the Si and reaches the bottom SiO_2

Device fabrication process (contd..)

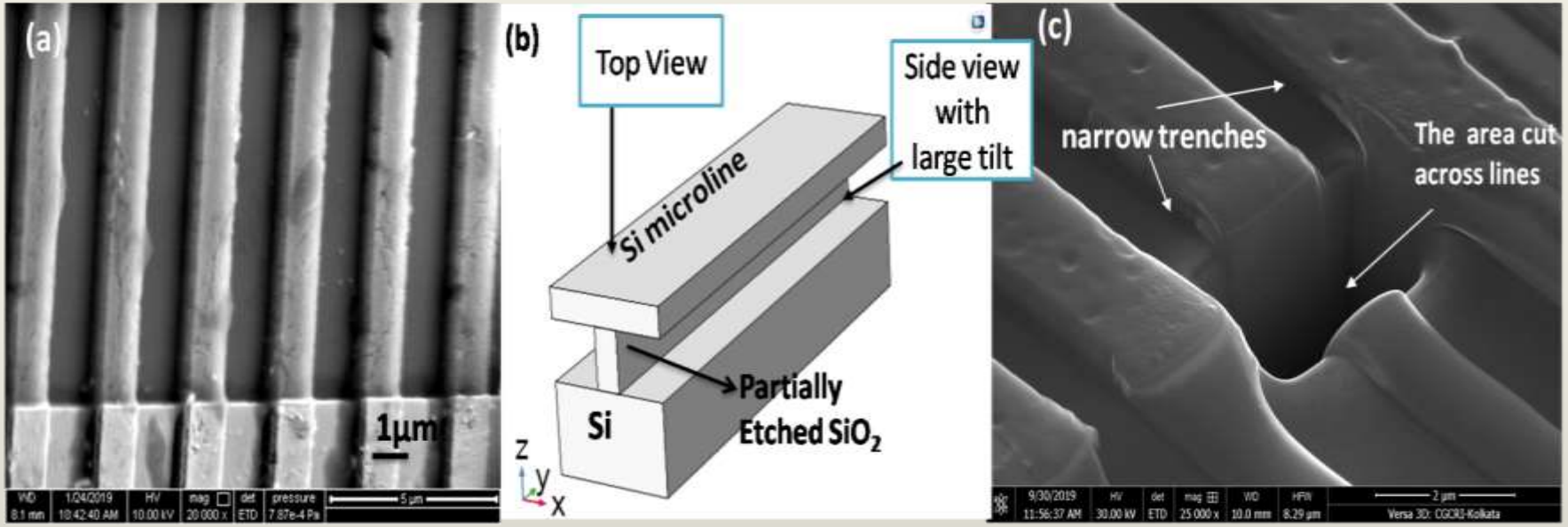


Partially suspended Si microlines

To make the structure partially suspended and to etch out the SiO_2 underneath Si microlines, we did a wet etching (acid etch) by dipping it in 20% Hydrofluoric acid (HF) solution.

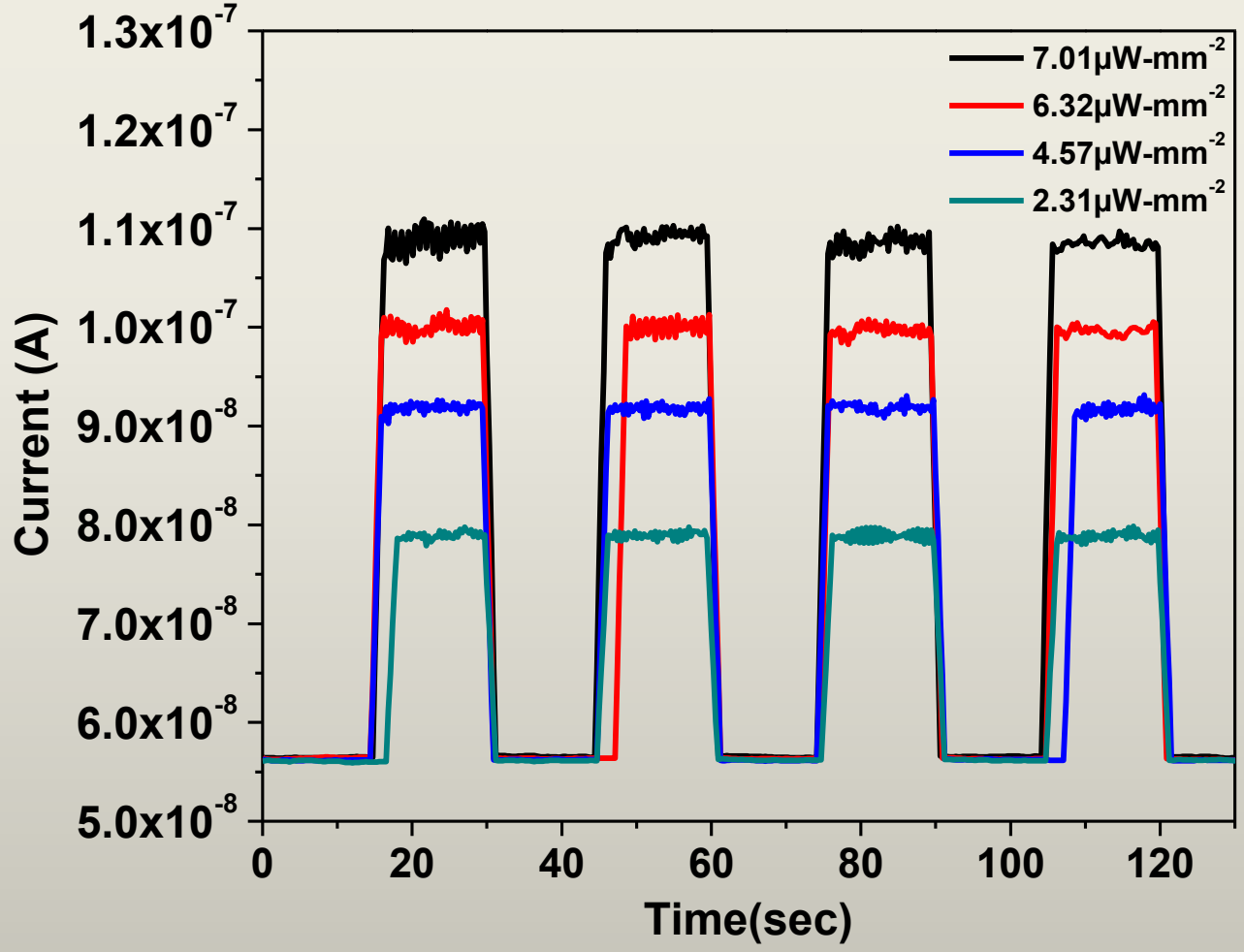


FESEM image of array of Si microlines

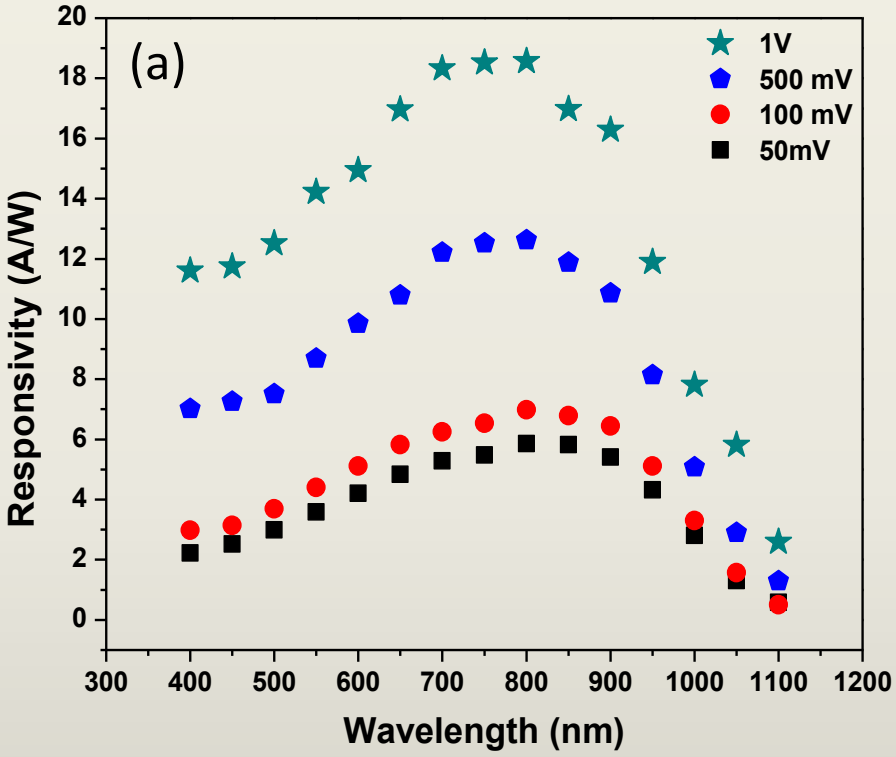


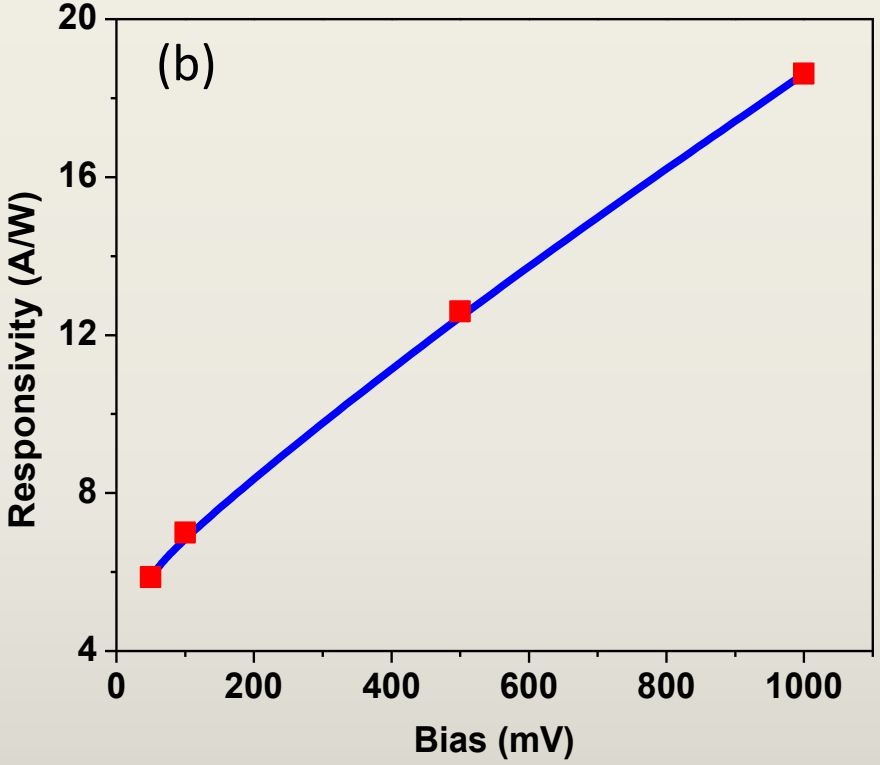
(a) FESEM image of array of Si microlines. (b) Schematic of the partially suspended device created by etching. The etching progressively removes the oxide under-layer on both sides and left behind a narrow strand that supports the microline. (c) Magnified view showing partially suspended Si microlines.

Photo Current vs. Time curve when light is turned ON/OFF



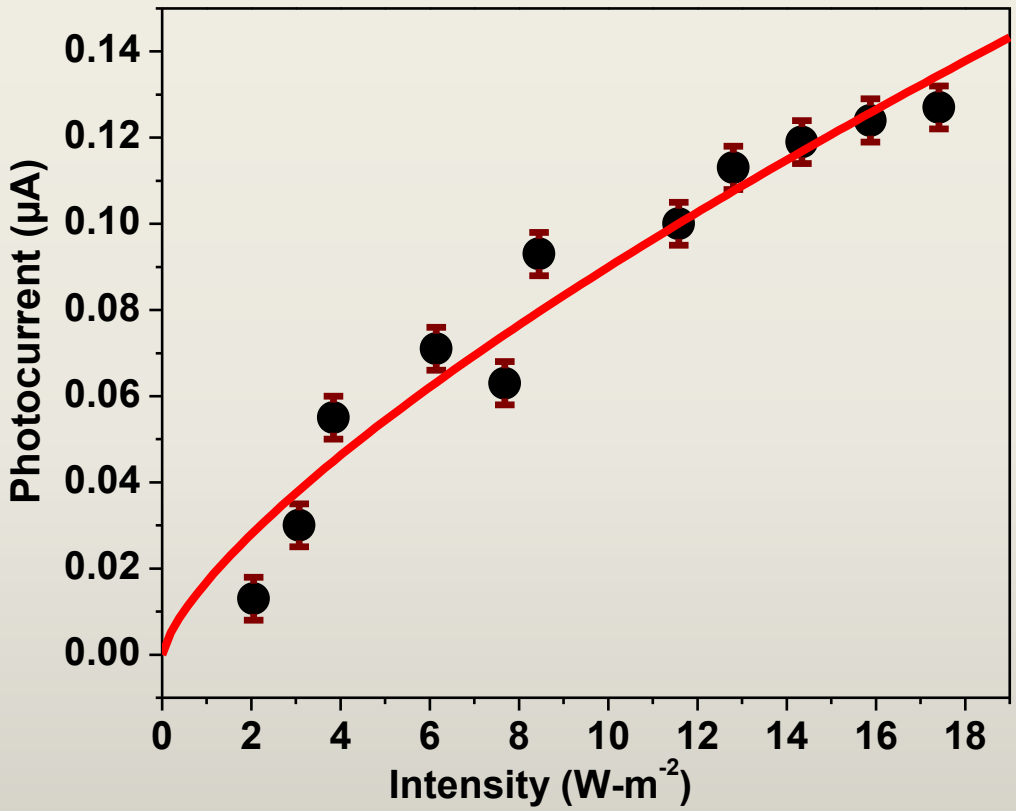
Responsivity vs. Wavelength





(a) Responsivity curve at different bias over a wavelength range of 400-1100 nm. (b) Peak Responsivity (λ=800nm) as function of bias.

Photocurrent vs. Intensity curve



As Power increases, Photocurrent increases because of enhancement of electron-hole pair density..!

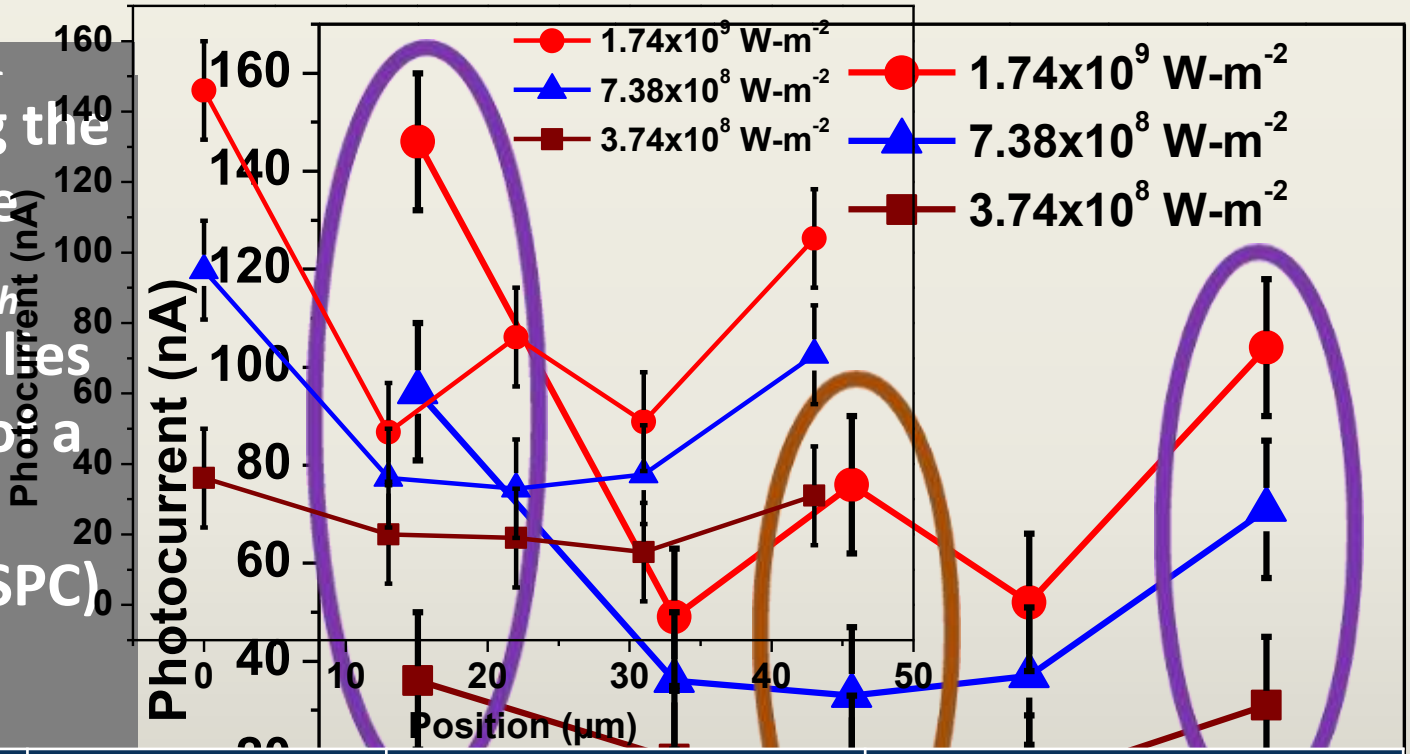
Power law fit

$$I_{ph} \propto J^{\alpha}$$

α = 0.72 (<1)
Trap states exists, depends on generation of electron-hole pairs, trapping and recombination of charge carriers in the device.

Photocurrent at different spots of device with varying intensity

On approaching the centre of the microline, I_{ph} decreases, implies characteristic of a Schottky Photocurrent (SPC) behavior



Intensity ($W\text{-}m^{-2}$)	I_{ph} at centre (nA)	Average I_{ph} at contact (nA)	Fraction of photocurrent
1.74×10^9	76	125	0.61
7.38×10^8	33	83	0.40
3.74×10^8	19	67	0.28

COMSOL Simulation

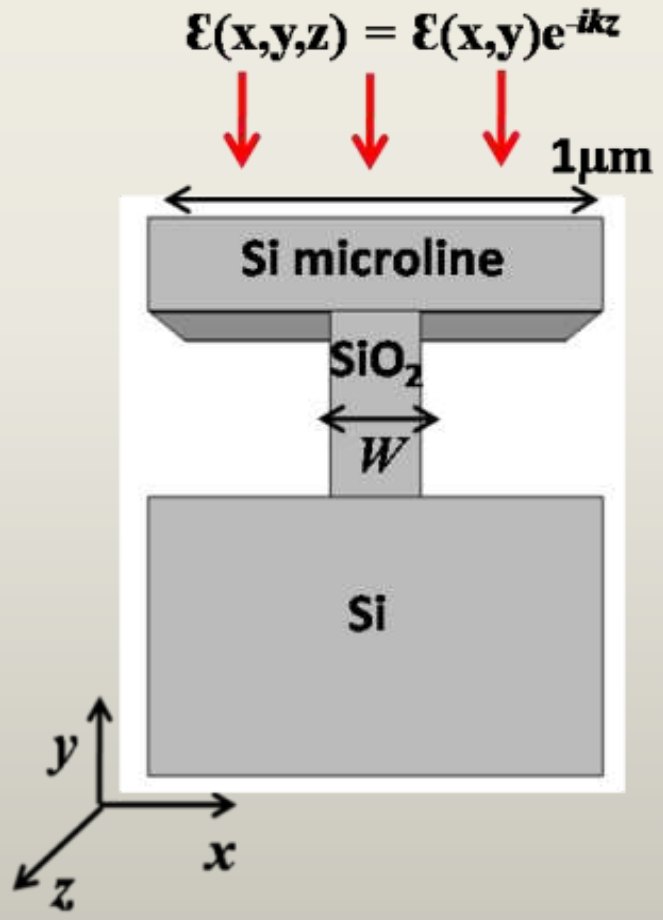
Physics we would like to address using COMSOL …??

Partial suspension of Si microline reduces the recombination pathways and increases the carrier lifetime which ultimately increases the responsivity of detector..!

Module Used

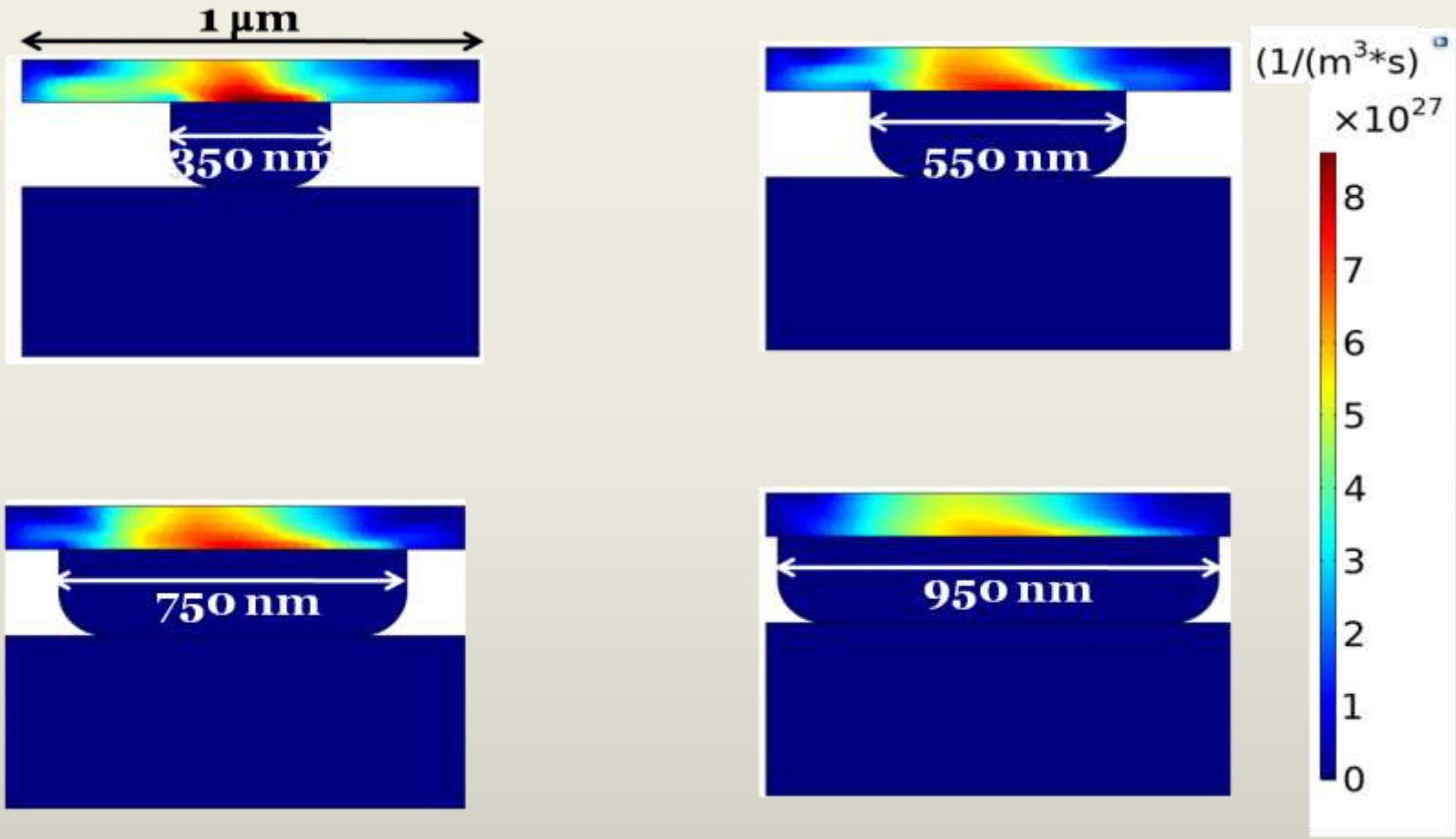
Semiconductor module coupled with electromagnetic wave module in frequency domain

COMSOL Simulation: Geometry used



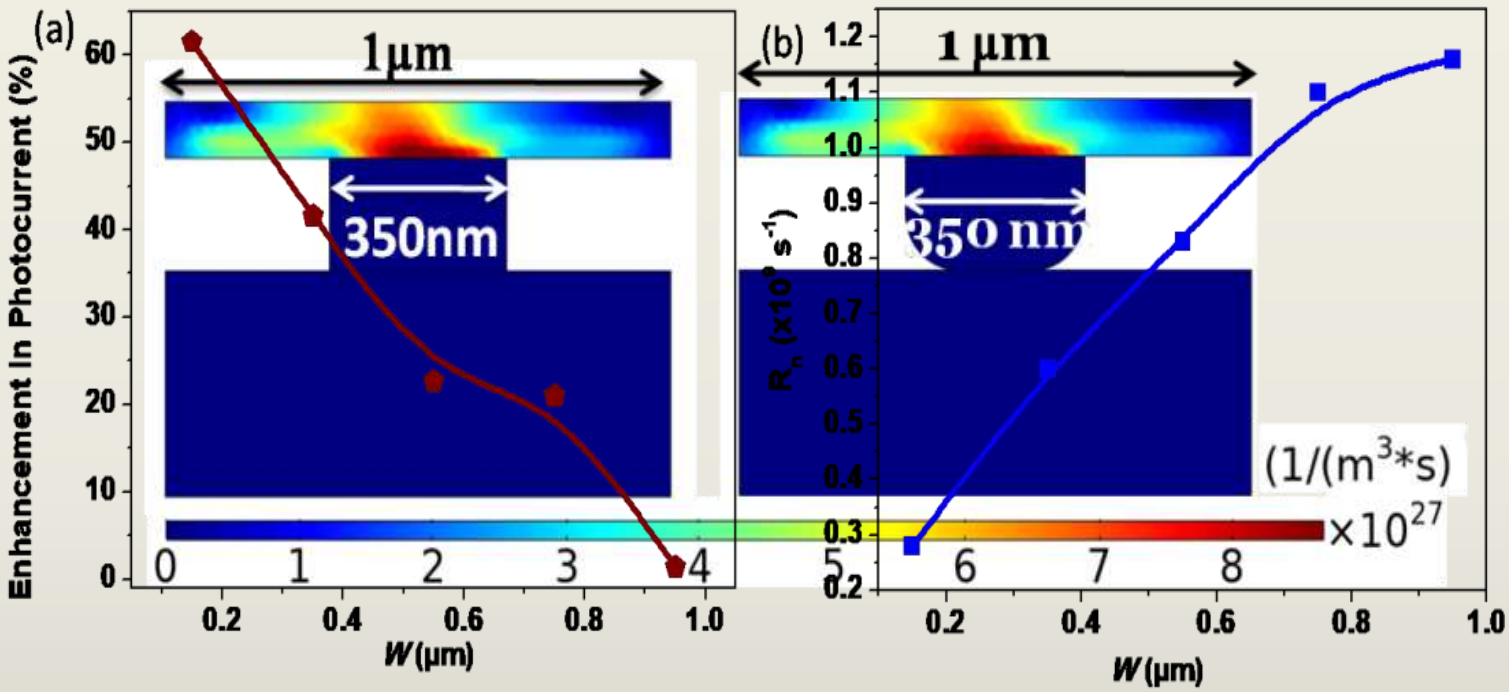
Cross-sectional image of device geometry of partially suspended Si microline used for simulation. The width *W* of the SiO_2 under-layer is a variable parameter in the simulation

COMSOL Simulation: Results



Surface plot of the carrier Recombination rate per unit volume in partially suspended Si microline with different width

COMSOL Simulation: Results



(a) Dependence of the enhancement of photocurrent (over dark current) and (b) carrier recombination rate R_n on the width W of the underlying SiO_2 layer that supports the microline

Surface plot of the carrier Recombination rate per unit volume in partially suspended Si microline with W=350 nm in sharp anisotropic etch profile and lateral etch profile

Conclusion

- We have developed a simple and useful technique for the fabrication of Silicon microlines from SOI wafer using a top-down method.

- The Responsivity is at least an order higher than commercially available bulk Si detectors in the same spectral range.

- The current in the device is controlled by trap states.

- Si microlines, which are partially suspended, prevent recombination of carriers during transit, thereby elongating its lifetime and has been validated by using COMSOL simulation.

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Thank You !!